



## KEYBOARD CONTROLLER

### GENERAL DESCRIPTION

The W83C42 keyboard controller is programmed to support the IBM® compatible personal computer keyboard serial interface. The keyboard controller receives serial data from the keyboard, checks the parity of the data, translates the scan code, and presents the data to the system as a byte of data in its output buffer. The controller will interrupt the system when data is placed in its output buffer. The byte of data will be sent to the keyboard serially with an odd parity bit automatically inserted. The keyboard is required to acknowledge all data transmissions. No transmission should be sent to the keyboard until acknowledgement is received for the previous byte sent.

Winbond Electronics Corporation has developed a fast keyboard controller and BIOS to improve the performance of IBM PC/AT® 386™ DX/SX and 486™ DX/SX machines and their compatibles. Hardwire methodology is used in this keyboard controller instead of software implementation, as in the traditional 8042 keyboard BIOS. This enables the keyboard controller to respond instantly to all commands sent from the keyboard to the CPU BIOS.

The keyboard controller enables popular programs such as AutoCAD®, Microsoft® Windows™ 3.1, NOVELL®, and other programs to run much faster.

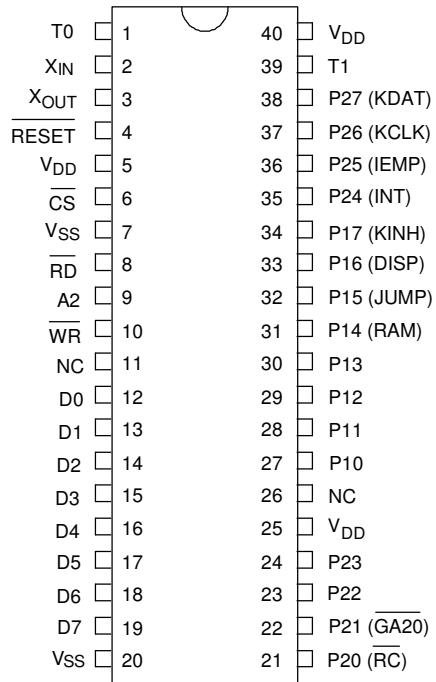
### FEATURES

- Supports IBM PC/AT 386DX/SX and 486 DX/SX system designs
- Runs much faster than traditional keyboard controllers
- Host interface compatible with traditional keyboard controller
- 6MHz~12MHz operating frequency
- Communicates with keyboard directly
- High-reliability CMOS technology
- Available packages: 40-pin DIP, 44-pin PLCC

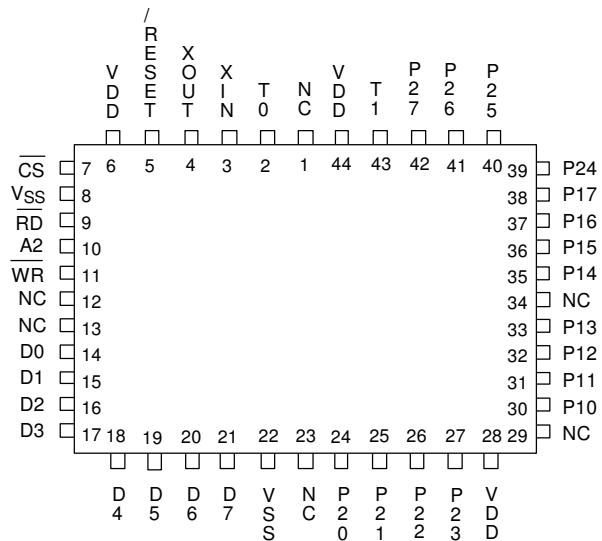
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## PIN CONFIGURATION

40-pin DIP



## 44-pin PLCC



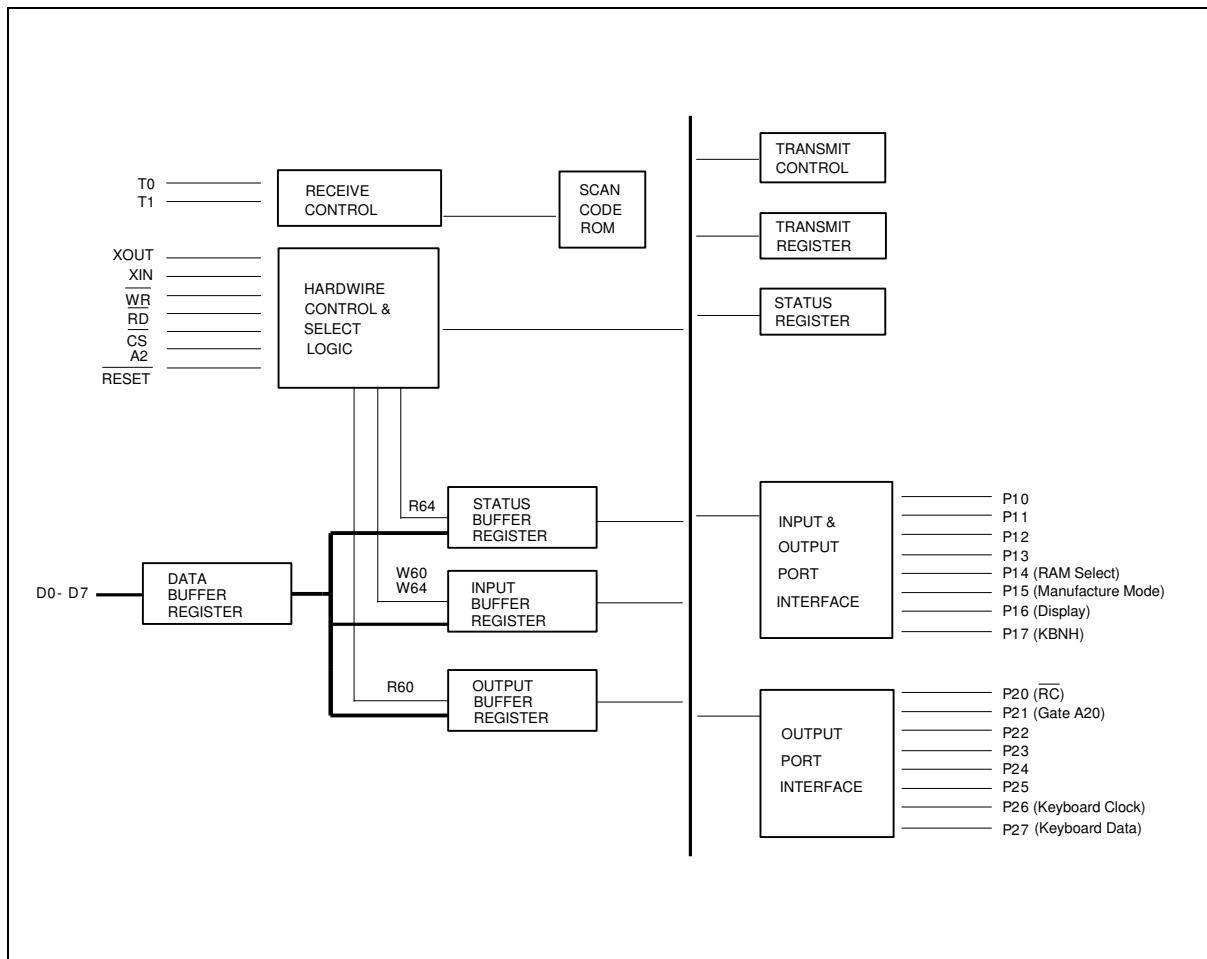
**PIN DESCRIPTION**

| PIN NO.<br>(40-pin DIP)              | PIN NO.<br>(44-pin PLCC)             | I/O | NAME         | FUNCTION                             |
|--------------------------------------|--------------------------------------|-----|--------------|--------------------------------------|
| 1                                    | 2                                    | I   | T0           | K/B Clock Input                      |
| 2                                    | 3                                    | I   | XIN          | Crystal Clock I/P                    |
| 3                                    | 4                                    | O   | XOUT         | Crystal Clock O/P                    |
| 4                                    | 5                                    | I   | <u>RESET</u> | Chip Reset                           |
| 5                                    | 6                                    | -   | VDD          | Optional +5V Power Supply            |
| 6                                    | 7                                    | I   | <u>CS</u>    | Chip Select                          |
| 7                                    | 8                                    | -   | Vss          | Optional Ground Power                |
| 8                                    | 9                                    | I   | <u>RD</u>    | I/O Read                             |
| 9                                    | 10                                   | I   | A2           | Connect to Address A2                |
| 10                                   | 11                                   | I   | <u>WR</u>    | I/O Write                            |
| 11, 26                               | 1, 12, 13,<br>23, 29, 34             | -   | NC           | Reserved                             |
| 12, 13, 14,<br>15, 16, 17,<br>18, 19 | 14, 15, 16,<br>17, 18, 19,<br>20, 21 | I/O | D0-D7        | Data Bus D0 - D7                     |
| 20                                   | 22                                   | -   | Vss          | Ground Power Supply                  |
| 21                                   | 24                                   | O   | P20          | Bit 0 of Port 2 (RCB: System Reset)  |
| 22                                   | 25                                   | O   | P21          | Bit 1 of Port 2 (GA20: GATE A20)     |
| 23                                   | 26                                   | I/O | P22          | Bit 2 of Port 2                      |
| 24                                   | 27                                   | I/O | P23          | Bit 3 of Port 2                      |
| 25                                   | 28                                   | -   | VDD          | Optional +5V Power Supply            |
| 27                                   | 30                                   | I/O | P10          | Bit 0 of Port 1                      |
| 28                                   | 31                                   | I/O | P11          | Bit 1 of Port 1                      |
| 29                                   | 32                                   | I/O | P12          | Bit 2 of Port 1                      |
| 30                                   | 33                                   | I/O | P13          | Bit 3 of Port 1                      |
| 31                                   | 35                                   | I   | P14          | Bit 4 of Port 1 (RAM Jumper Select)  |
| 32                                   | 36                                   | I   | P15          | Bit 5 of Port 1 (JUMP)               |
| 33                                   | 37                                   | I   | P16          | Bit 6 of Port 1 (Display Select)     |
| 34                                   | 38                                   | I   | P17          | Bit 7 of Port 1 (K/B Inhibit Switch) |

## Pin Description, continued

| PIN NO.<br>(40-pin DIP) | PIN NO.<br>(44-pin PLCC) | I/O | NAME | FUNCTION                            |
|-------------------------|--------------------------|-----|------|-------------------------------------|
| 35                      | 39                       | O   | P24  | Bit 4 of Port 2 (OBF O/P Interrupt) |
| 36                      | 40                       | O   | P25  | Bit 5 of Port 2 (I/P Buffer Empty)  |
| 37                      | 41                       | O   | P26  | Bit 6 of Port 2 (K/B Clock O/P)     |
| 38                      | 42                       | O   | P27  | Bit 7 of Port 2 (K/B Data O/P)      |
| 39                      | 43                       | I   | T1   | K/B Data Input                      |
| 40                      | 44                       | -   | VDD  | +5V Power Supply                    |

## BLOCK DIAGRAM

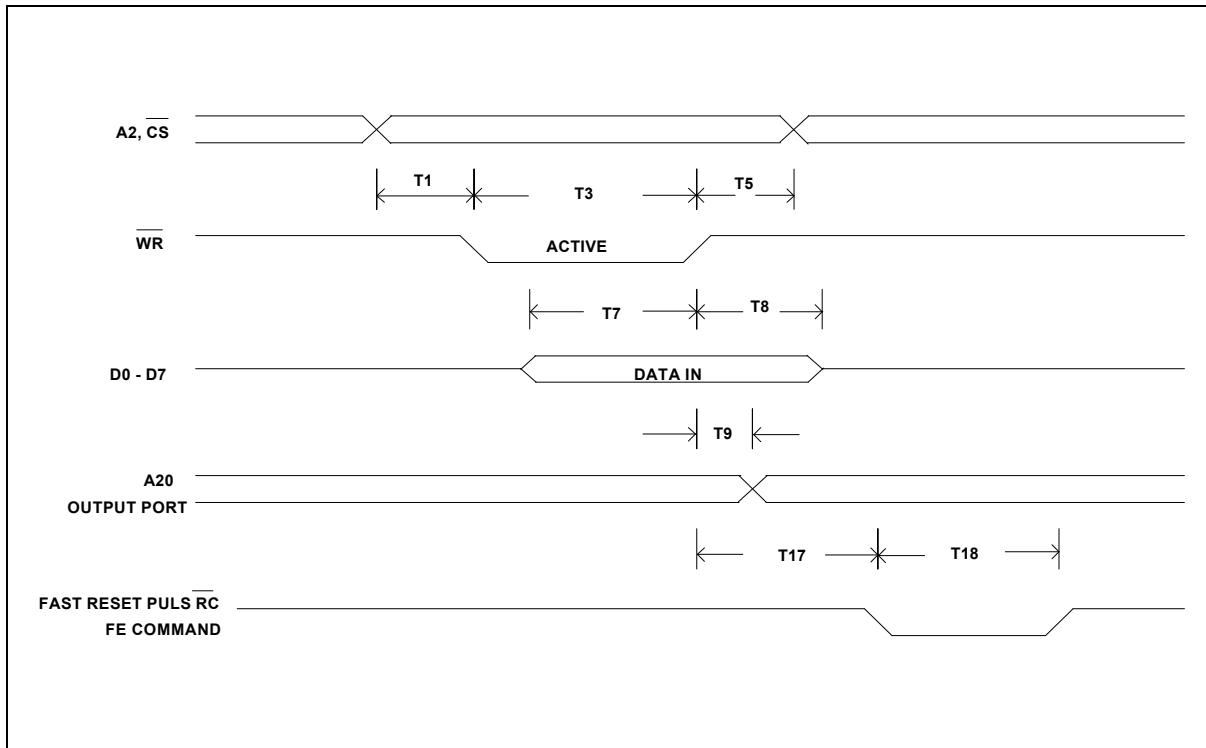


**AC TIMING**

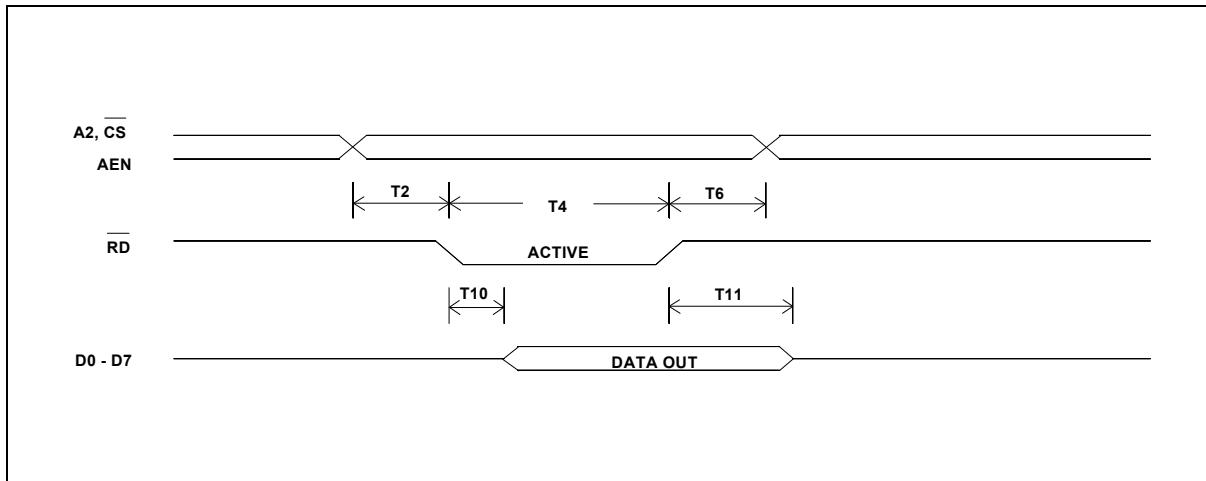
| NO. | DESCRIPTION                               | MIN. | MAX. | UNIT |
|-----|---|------|------|------|
| T1  | Address Setup Time from WR                | 0    |      | nS   |
| T2  | Address Setup Time from RD                | 0    |      | nS   |
| T3  | WR Strobe Width                           | 20   |      | nS   |
| T4  | RD Strobe Width                           | 20   |      | nS   |
| T5  | Address Hold Time from WR                 | 0    |      | nS   |
| T6  | Address Hold Time from RD                 | 0    |      | nS   |
| T7  | Data Setup Time                           | 50   |      | nS   |
| T8  | Data Hold Time                            | 0    |      | nS   |
| T9  | Gate Delay Time from WR                   | 10   |      | nS   |
| T10 | RD to Drive Data Delay                    |      | 20   | nS   |
| T11 | RD to Floating Data Delay                 | 0    | 20   | nS   |
| T12 | Data Valid After Clock Falling (SEND)     |      | 4    | μS   |
| T13 | K/B Clock Period                          | 20   |      | μS   |
| T14 | K/B Clock Pulse Width                     | 10   |      | μS   |
| T15 | Data Valid Before Clock Falling (RECEIVE) | 4    |      | μS   |
| T16 | K/B ACK After Finish Receiving            | 20   |      | μS   |
| T17 | RC Fast Reset Pulse Delay (8 MHz)         | 2    | 3    | μS   |
| T18 | RC Pulse Width (8 MHz)                    | 6    |      | μS   |
| T19 | Transmit Timeout                          |      | 2    | mS   |
| T20 | Data Valid Hold Time                      | 0    |      | μS   |
| T21 | XIN/XOUT Period ( 6-12 MHz )              | 83   | 167  | nS   |

## TIMING WAVEFORMS

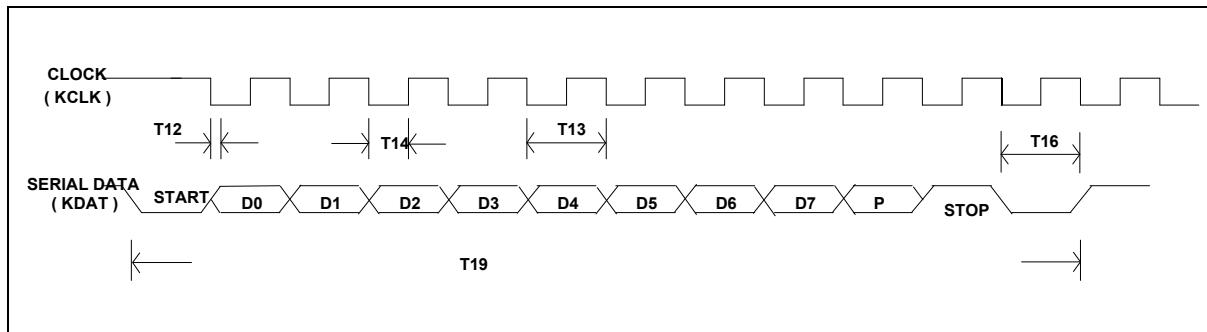
### Write Cycle Timing



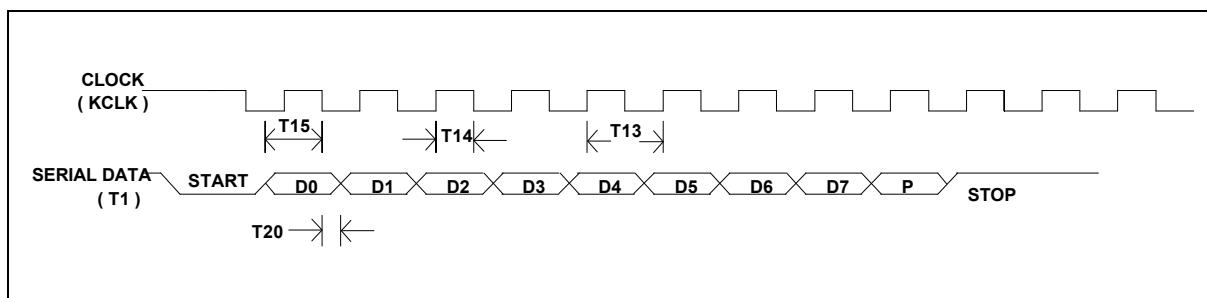
### Read Cycle Timing



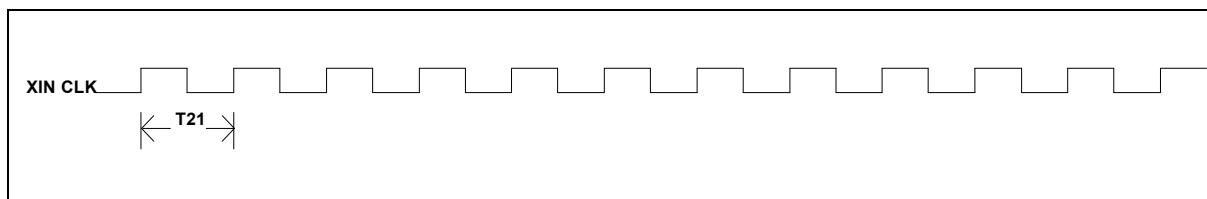
## Send Data to K/B



## Receive Data from K/B



## XIN/XOUT Clock



## ABSOLUTE MAXIMUM RATINGS

| PARAMETER                          | RATING       | UNIT |
|------------------------------------|--------------|------|
| Ambient Operating Temperature      | -0 to +85    | °C   |
| Storage Temperature                | -65 to +150  | °C   |
| Supply Voltage to Ground Potential | -0.3 to +7.0 | V    |
| Applied Input/Output Voltage       | -0.3 to +7.0 | V    |
| Power Dissipation                  | 50           | mW   |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

## ELECTRICAL CHARACTERISTICS & CAPACITANCE

(Ta = 0° C to +70° C, VDD = +5V ±5%)

| SYMBOL | DESCRIPTION                            | MIN.     | TYP. | MAX. | UNIT |
|--------|--|----------|------|------|------|
| VDD    | Power Supply                           | 4.75     | 5.0  | 5.25 | V    |
| TA     | Operating Temperature                  | 0        | 25   | 70   | V    |
| VIH    | High Level Voltage for TTL<br>Min. I/P | 2.0      |      | VDD  | V    |
| VIL    | Low Level Voltage for TTL<br>Max. I/P  | -0.3     |      | 0.8  | V    |
| VOH    | High Level Voltage for TTL<br>Min. O/P | VDD -0.5 |      |      | V    |
| VOL    | Low Level Voltage for TTL<br>Max. O/P  |          |      | 0.5  | V    |
| RIP    | Min. I/P Resist                        | 10K      |      |      | Ω    |
| ILI    | I/P Leakage Current                    | -10      |      | 10   | μA   |
| ILO    | O/P Leakage Current                    | -10      |      | 10   | μA   |
| IOL    | O/P Sink Current                       | 4        |      |      | mA   |
| CL     | O/P Load Capacity                      | 15       |      | 50   | pF   |

## STATUS REGISTER

The status register is an 8-bit read-only register at I/O address hex 64 that holds information about the state of the keyboard controller and interface. It may be read at any time.

| BIT | BIT DESCRIPTION    | FUNCTION  |
|-----|--------------------|---|
| 0   | Output Buffer Full | 0: Output Buffer Empty<br>1: Output Buffer Full   |
| 1   | Input Buffer Full  | 0: Input Buffer Empty<br>1: Input Buffer Full   |
| 2   | System Flag        | This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller. It is set to 0 after a power-on reset |
| 3   | Command/data       | 0: Data Byte<br>1: Command Byte   |
| 4   | Inhibit Switch     | 0: Keyboard is Inhibited<br>1: Keyboard is Not Inhibited  |
| 5   | Transmit Time Out  | 0: No Transmit Time Out Error<br>1: Transmit Time Out Error   |



Status Register, continued

| BIT | BIT DESCRIPTION  | FUNCTION  |
|-----|------------------|---|
| 6   | Receive Time Out | 0: No Receive Time Out Error<br>1: Receive Time Out Error |
| 7   | Parity Error     | 0: Odd Parity (No Error)<br>1: Even Parity (Error)        |

## OUTPUT BUFFER

The output buffer is an 8-bit read-only register at I/O address hex 60. The keyboard controller uses the output buffer to send the scan code received from the keyboard and data bytes required by command to the system. The output buffer should be read only when the output buffer full bit in the register is 1.

## INPUT BUFFER

The input buffer is an 8-bit write-only register at I/O address hex 60 or 64. Writing to address hex 60 sets a flag that indicates a data write; writing to address hex 64 sets a flag that indicates a command write. Data written to I/O address hex 60 are sent to the keyboard (unless the keyboard controller is expecting a data byte) following the controller's input buffer only if the input buffer full bit in the status register is set to 0.

## I/O PORTS

The keyboard controller has two 8-bit I/O ports and two test inputs. One of the ports is assigned for input and the other for output. The controller uses the test inputs to read the state of the keyboard's clock line and data line.

The following figures show bit definitions for the input, output, and test-input ports.

### (A) Input Port Definitions

| BIT | FUNCTION   |
|-----|--|
| 0   | Undefined  |
| 1   | Undefined  |
| 2   | Undefined  |
| 3   | Undefined  |
| 4   | RAM on System Board<br>0: Disable 2nd 256 KB of System Board RAM<br>1: Enable 2nd 256 KB of System Board RAM |
| 5   | Manufacturing Jumper Installed<br>0: Manufacturing Jumper<br>1: Jumper Not Installed                         |



## Input Port Definitions, continued

| BIT | FUNCTION  |
|-----|---|
| 6   | Display Type Switch<br>0: Primary Display Attached to Color/graphics<br>0: Primary Display Attached to Monochrome |
| 7   | Keyboard Inhibit Switch<br>0: Keyboard Inhibited<br>1: Keyboard Not Inhibited                                     |

**(B) Output Port Definitions**

| BIT | FUNCTION                |
|-----|-------------------------|
| 0   | System Reset            |
| 1   | Gate A20                |
| 2   | Undefined               |
| 3   | Undefined               |
| 4   | Output Buffer Full      |
| 5   | Input Buffer Empty      |
| 6   | Keyboard Clock (Output) |
| 7   | Keyboard Data (Output)  |

**(C) Test-Input Definitions**

| BIT | FUNCTION               |
|-----|------------------------|
| 0   | Keyboard Clock (Input) |
| 1   | Keyboard Data (Input)  |

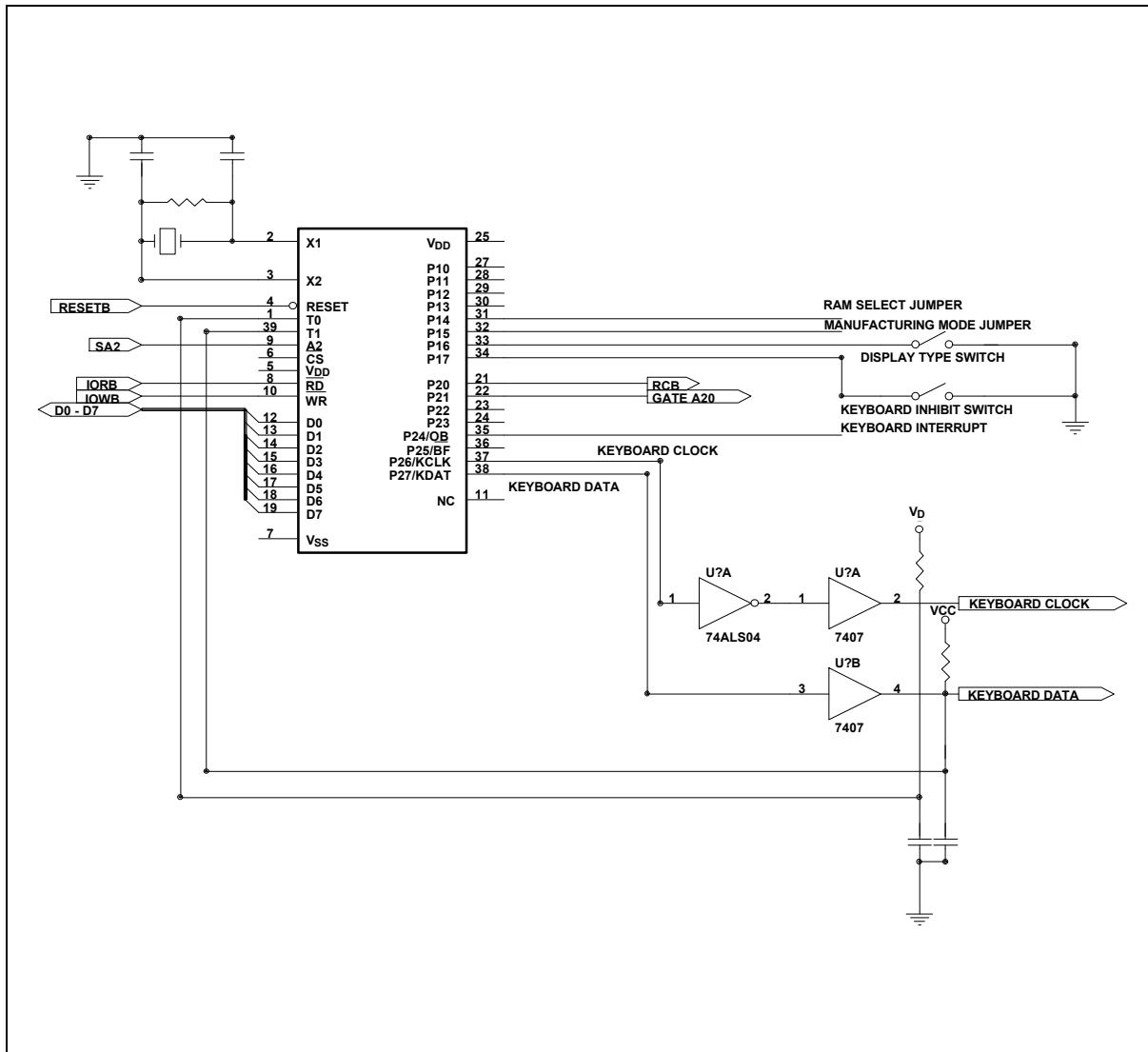


## COMMANDS (I/O ADDRESS HEX 64)

| COMMAND | FUNCTION  |    |                   |    |                             |    |                              |    |                            |    |                             |   |             |   |          |   |                                     |
|---------|---|----|-------------------|----|-----------------------------|----|------------------------------|----|----------------------------|----|-----------------------------|---|-------------|---|----------|---|-------------------------------------|
| 20      | Read Command Byte of Keyboard Controller  |    |                   |    |                             |    |                              |    |                            |    |                             |   |             |   |          |   |                                     |
| 60      | <p>Write Command Byte of Keyboard Controller</p> <p><b>BIT      BIT DEFINITIONS</b></p> <table> <tr> <td>7</td><td>Reserved</td></tr> <tr> <td>6</td><td>IBM PC Compatible Mode</td></tr> <tr> <td>5</td><td>IBM PC Mode</td></tr> <tr> <td>4</td><td>Disable Keyboard</td></tr> <tr> <td>3</td><td>Inhibit Override</td></tr> <tr> <td>2</td><td>System Flag</td></tr> <tr> <td>1</td><td>Reserved</td></tr> <tr> <td>0</td><td>Enable Output Buffer Full Interrupt</td></tr> </table> | 7  | Reserved          | 6  | IBM PC Compatible Mode      | 5  | IBM PC Mode                  | 4  | Disable Keyboard           | 3  | Inhibit Override            | 2 | System Flag | 1 | Reserved | 0 | Enable Output Buffer Full Interrupt |
| 7       | Reserved  |    |                   |    |                             |    |                              |    |                            |    |                             |   |             |   |          |   |                                     |
| 6       | IBM PC Compatible Mode  |    |                   |    |                             |    |                              |    |                            |    |                             |   |             |   |          |   |                                     |
| 5       | IBM PC Mode   |    |                   |    |                             |    |                              |    |                            |    |                             |   |             |   |          |   |                                     |
| 4       | Disable Keyboard  |    |                   |    |                             |    |                              |    |                            |    |                             |   |             |   |          |   |                                     |
| 3       | Inhibit Override  |    |                   |    |                             |    |                              |    |                            |    |                             |   |             |   |          |   |                                     |
| 2       | System Flag   |    |                   |    |                             |    |                              |    |                            |    |                             |   |             |   |          |   |                                     |
| 1       | Reserved  |    |                   |    |                             |    |                              |    |                            |    |                             |   |             |   |          |   |                                     |
| 0       | Enable Output Buffer Full Interrupt   |    |                   |    |                             |    |                              |    |                            |    |                             |   |             |   |          |   |                                     |
| AA      | <p>Self-test</p> <p><b>BIT      BIT DEFINITIONS</b></p> <table> <tr> <td>00</td><td>No Error Detected</td></tr> <tr> <td>01</td><td>K/B Clock Line is Stuck Low</td></tr> <tr> <td>02</td><td>K/B Clock Line is Stuck High</td></tr> <tr> <td>03</td><td>K/B Data Line is Stuck Low</td></tr> <tr> <td>04</td><td>K/B Data Line is Stuck High</td></tr> </table>  | 00 | No Error Detected | 01 | K/B Clock Line is Stuck Low | 02 | K/B Clock Line is Stuck High | 03 | K/B Data Line is Stuck Low | 04 | K/B Data Line is Stuck High |   |             |   |          |   |                                     |
| 00      | No Error Detected   |    |                   |    |                             |    |                              |    |                            |    |                             |   |             |   |          |   |                                     |
| 01      | K/B Clock Line is Stuck Low   |    |                   |    |                             |    |                              |    |                            |    |                             |   |             |   |          |   |                                     |
| 02      | K/B Clock Line is Stuck High  |    |                   |    |                             |    |                              |    |                            |    |                             |   |             |   |          |   |                                     |
| 03      | K/B Data Line is Stuck Low  |    |                   |    |                             |    |                              |    |                            |    |                             |   |             |   |          |   |                                     |
| 04      | K/B Data Line is Stuck High   |    |                   |    |                             |    |                              |    |                            |    |                             |   |             |   |          |   |                                     |
| AB      | Interface Test  |    |                   |    |                             |    |                              |    |                            |    |                             |   |             |   |          |   |                                     |
| AD      | Disable Keyboard Feature  |    |                   |    |                             |    |                              |    |                            |    |                             |   |             |   |          |   |                                     |
| AE      | Enable Keyboard Interface   |    |                   |    |                             |    |                              |    |                            |    |                             |   |             |   |          |   |                                     |
| C0      | Read Input Port   |    |                   |    |                             |    |                              |    |                            |    |                             |   |             |   |          |   |                                     |
| D0      | Read Output Port  |    |                   |    |                             |    |                              |    |                            |    |                             |   |             |   |          |   |                                     |
| D1      | Write Output Port   |    |                   |    |                             |    |                              |    |                            |    |                             |   |             |   |          |   |                                     |
| E0      | Read Test Inputs  |    |                   |    |                             |    |                              |    |                            |    |                             |   |             |   |          |   |                                     |
| F0-FF   | Pulse Output Port   |    |                   |    |                             |    |                              |    |                            |    |                             |   |             |   |          |   |                                     |

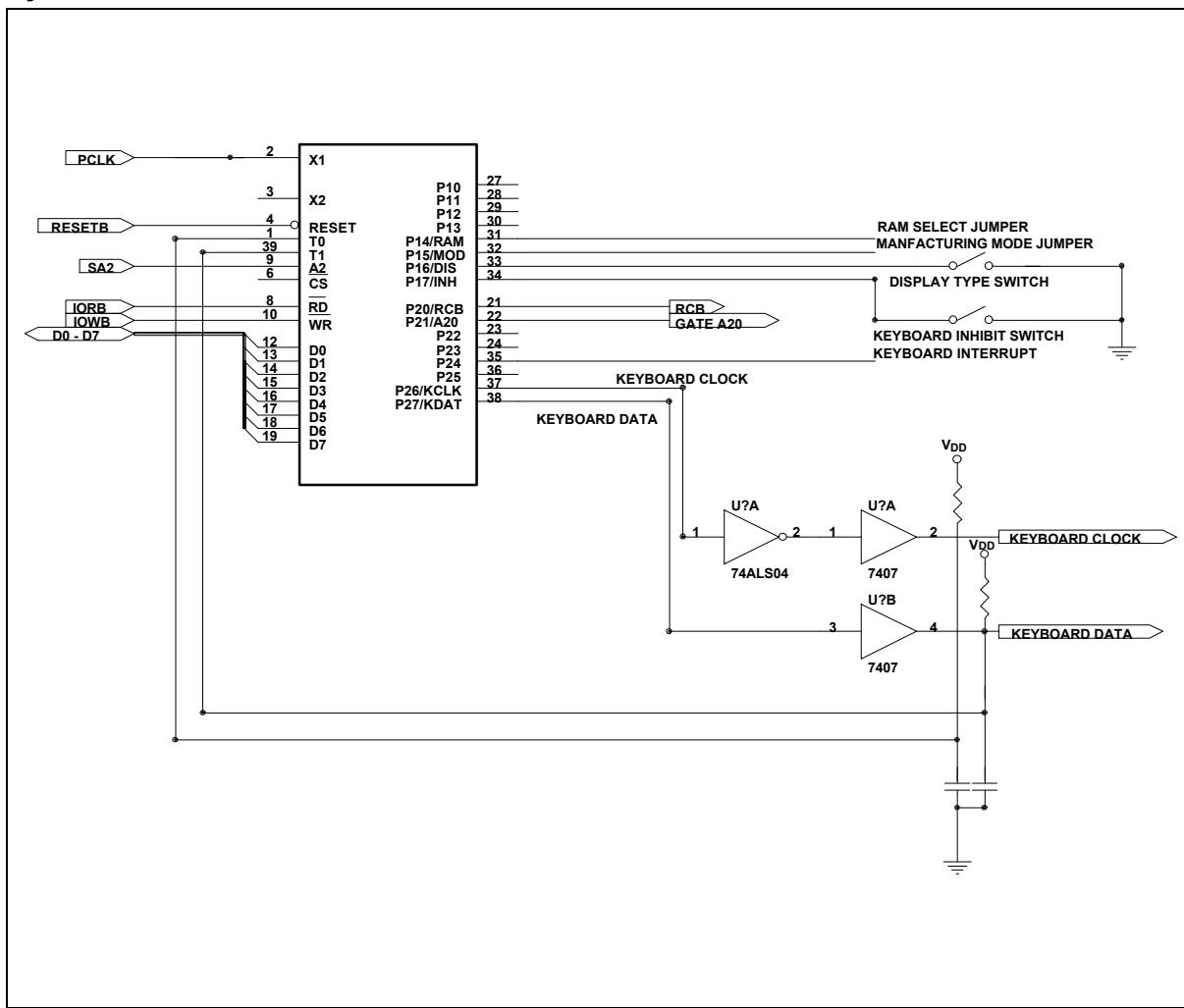
## APPLICATION CIRCUIT

### Asynchronous



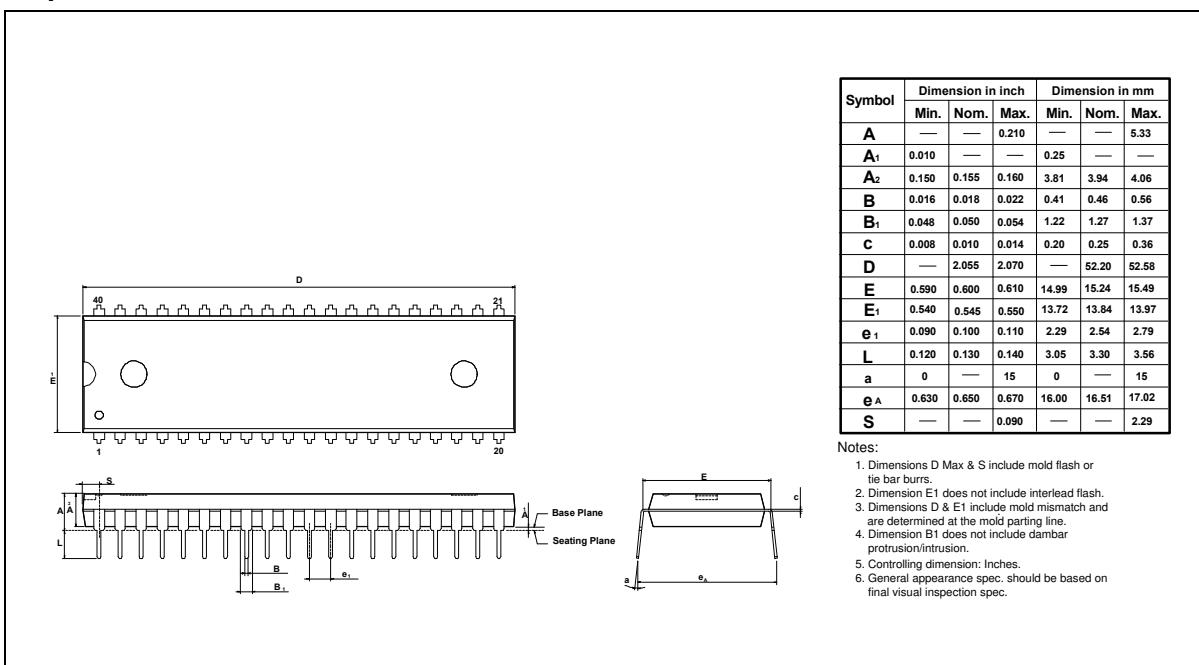
Application Circuit, continued

## Synchronous

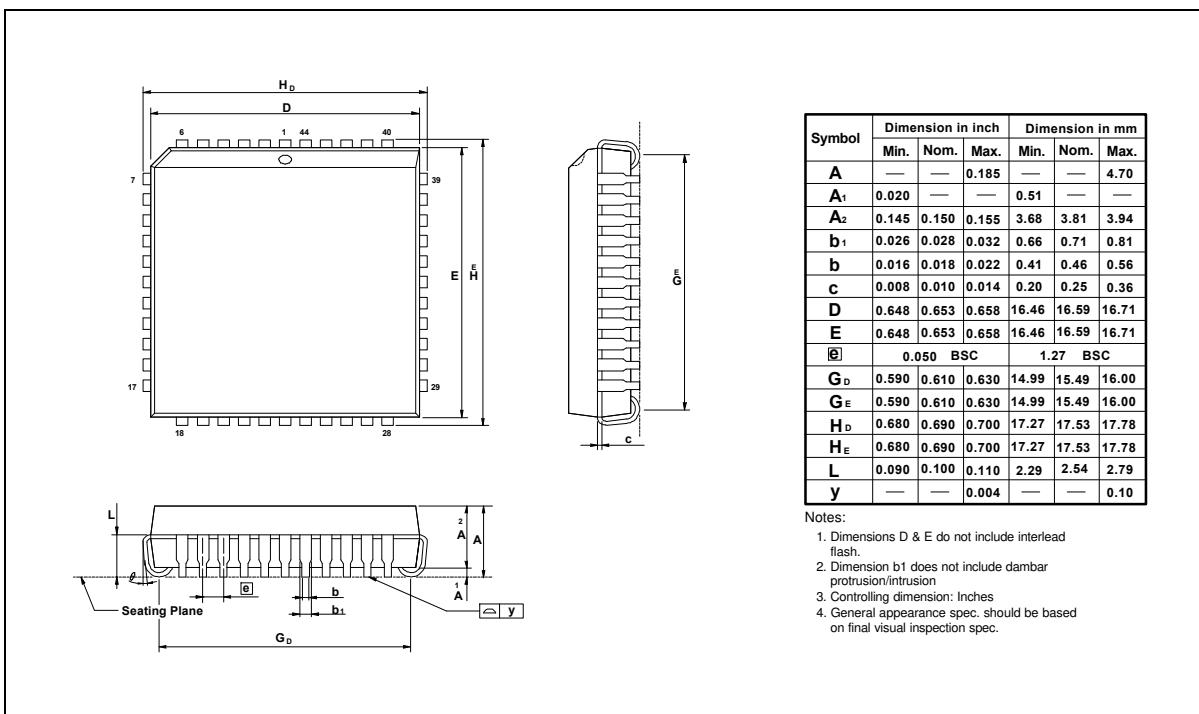


## PACKAGE DIMENSIONS

### 40-pin PDIP



### 44-pin PLCC





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Note: All data and specifications are subject to change without notice.